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Solid state storage **device** - all 2 versions »
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Storage **device** having varying access times and a superscalar microprocessor employing the same - all 3 versions »
TM Tran... - US Patent 5,900,012, 1999 - Google Patents
... equal to a respective number of high order **bits** of ... hold register 62 provide a temporary storage **device** for a ... line for the case where a request **address** misses ...
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... been searched (the logical 1 **bit** is again in position 1 ... a symbolic ad -dress and a physical **address** for pages of data stored in the **device**, each register ...
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RG Fleck, K Oberlaender, G Baror, A Eder - US Patent 6,405,273, 2002 - Google Patents
... (54) DATA PROCESSING **DEVICE** WITH MEMORY ... A memory having a plurality of n-**bit**
input/output ports ... the memory with the register file, a memory **address** and select ...
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TM Austin, GS Sohi - ISCA, 1996 - minds.wisconsin.edu
... banks, and hence, the band- width delivered by the **device**. In our evaluations, we consider both **bit** selection, which ... a portion of the virtual page **address** to se ...
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Display apparatus and method capable of rotating an image by 180 degrees - all 6 versions »
B Cheng - US Patent 6,765,581, 2004 - Google Patents
... Based on the orientation ol a display **device**, a **address** translation system either passes the software **address** "as is" or translates the **address** to represent a ...
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... pixel height and W 0 is the landscape-oriented display **device** pixel width. L represents the number of least significant software **address bits** to translate as ...
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Reorder buffer employing last in buffer and last in line bits - all 2 versions »
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... I/O **Device** I/O **Device** FIG. 10 208 ... Microprocessors which implement out of order execution
BUFFER AND LAST IN LINE **BITS** often employ a **reorder** buffer for ...
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T Bhm, H Kandolf, S Lammers, Z Manyoki - US Patent 6,618,306, 2003 - Google Patents
... **device**, only when the first control **bit** has a given first binary value, setting a first operating state in which the **address** decoding **device** uses **bits** of all ...
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... 2. The **device** of claim 1 wherein said **reorder** circuit is configured for examining at least two ofthe least significant **bits** of a column **address** and wherein ...
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... conditions, processor order" by the decoder as allowed by the **reorder** buffer, states, and the **address** of the current instruction to In ...
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... register files, instruction dispatch buffers, **re–order** buffers, as well ... units or moved into the **reorder** and dispatch ... with the use of **bit**–value invariances ...
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J González, A González - Proc. of EURO-PAR 97 Workshop on ILP, 1997 - ac.upc.edu
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A Bhatt, A Dhanotia, MD CharuSachdeva, N Choudary, ... - cadence.co.in
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... Ifthe valid **bit** is set for the cell corresponding to Rptr, **reorder** engine 322 processes that cell by outputting the cell **address** for the cell (acts 603 and ...
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